Sagar Bhaveshkumar Patel

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Summary

Embedded Systems Engineer with 4+ years of experience designing high-performance networking firmware and intelligent edge platforms across telecom, carrier networking, and logistics infrastructure. Expertise in embedded Linux, packet processing pipelines, RTOS and device driver development, and secure firmware for ARM-based systems. Proven ability to optimize system throughput, reliability, and deterministic performance while integrating AI-powered edge computing on NVIDIA platforms to deliver scalable, production-grade embedded and data-plane systems.

Technical Skills

Programming Languages: C, C++, Python, Bash
Embedded Systems & Firmware: Embedded software development, bare-metal programming, RTOS-based systems, device driver development, BSP integration, interrupt handling, memory management, bootloader development, firmware debugging and optimization
Networking & Data Plane: TCP/IP, Ethernet switching and routing, Layer 2/Layer 3 networking, packet processing pipelines, DMA optimization, QoS and traffic shaping, multicast networking, network telemetry
Embedded Linux: Embedded Linux kernel configuration, kernel modules, Yocto, Buildroot, cross-compilation toolchains, device tree configuration, IPC mechanisms
Edge AI & NVIDIA Platforms: CUDA, TensorRT, cuDNN, ONNX, NVIDIA Jetson (Xavier, Orin), JetPack SDK, DeepStream, Nsight Systems
Security & Reliability: Secure boot, firmware authentication, cryptographic integration, MISRA-C compliance, static analysis, JTAG debugging, fault injection and stress testing, CI/CD for embedded systems
Hardware & Platforms: ARM-based embedded systems, NVIDIA Jetson platforms, NVIDIA BlueField DPUs, PCIe, DMA engines, high-speed Ethernet interfaces

Professional Experience

Embedded Software Engineer, *Ciena* May 2024 – Present | Remote, USA

- Engineered embedded Linux networking firmware for logistics edge gateways, optimizing packet processing pipelines, DMA transfer paths, and interrupt handling to improve sustained throughput by 31% during peak fulfillment operations.
- Led development and maintenance of the embedded Linux platform using Yocto, performing BSP upgrades, secure boot integration, CI validation, and release management, reducing hardware bring-up and deployment timelines by 24%.
- Implemented system reliability mechanisms including watchdog recovery, failover handling, and deterministic latency validation under varying power, thermal, and network conditions.
- Developed edge AI inference pipelines on NVIDIA Jetson Orin using CUDA and TensorRT to detect conveyor and sorter anomalies in real time, reducing unplanned operational downtime by 22%.
- Built DeepStream-based video and telemetry pipelines integrating multi-sensor data streams, improving fault localization accuracy by 27% during high-throughput warehouse processing.
- Conducted GPU and system-level profiling using NVIDIA Nsight Systems to analyze memory bandwidth and kernel execution, optimizing AI inference pipelines and networking tasks to maintain deterministic latency and stable throughput under production traffic.

Embedded Software Engineer, *CISCO Systems Inc.* Jan 2023 – Apr 2024 | Austin, TX

- Engineered switching firmware integrating P4-programmable data-plane pipelines with switching ASIC SDKs, improving forwarding stability and reducing packet loss by 31% during large-scale network validation.
- Developed embedded Linux platform components using Yocto, including secure boot configuration, telemetry drivers, and CI pipelines, accelerating multi-router platform readiness by 21% for carrier certification.
- Implemented AI-assisted traffic intelligence using NVIDIA BlueField DPUs, integrating DOCA pipelines and ONNX inference models to improve encrypted anomaly classification accuracy by 24%.
- Integrated real-time inference with streaming gRPC telemetry pipelines, enabling predictive congestion detection and reducing root-cause analysis time by 34% across distributed carrier networks.
- Optimized DPU offload scheduling and inference workloads through DOCA profiling tools, reducing host CPU utilization by 29% while maintaining stable throughput under peak traffic conditions.

Embedded Software Engineer, *TCS* Jul 2020 – Aug 2021 | Remote, India

- Developed bare-metal RTOS firmware for ARM-based telecom edge nodes, implementing multicast packet replication and QoS traffic shaping to boost reliable delivery rates by 28% under bursty carrier loads.
- Wrote custom kernel modules and device drivers for high-speed Ethernet interfaces, enabling efficient memory management and DMA engines that cut packet jitter by 35% in distributed network deployments.
- Integrated bootloader development with firmware authentication and MISRA-C compliant coding, streamlining secure deployment across multi-vendor platforms and advancing field rollout by 18 days.
- Optimized Layer 2/3 networking stacks with fault injection testing and JTAG debugging, enhancing protocol stability and reducing error rates by 26% during stress-tested edge scenarios.
- Configured Embedded Linux using Buildroot and device tree overlays for real-time IPC mechanisms, improving cross-process coordination and cutting synchronization overhead by 32% in carrier-grade environments.

Certificate

NVIDIA-Certified Associate: Generative AI LLMs

Education

Master of Science in Computer Science, *Sofia University* Oct 2025 – Jun 2027 | CA, USA
Master of Embedded and Cyber Physical Systems, *University of California Irvine* Sep 2021 – Dec 2022 | CA, USA
Bachelor of Technology, *Charotar University of Science and Technology* Jul 2017 – Jun 2021 | Gujarat, India